AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (original): An organic insulating film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 2 (original): An organic insulating film according to Claim 1, wherein said polyorganosilane is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane, tetravinylsilane, tetraethylsilane and triethylsilane.

Claim 3 (original): An organic insulating film according to Claim 1, wherein said polyorganosilane contains a vinyl group, at least, in a part thereof.

Claim 4 (original): An organic insulating film according to Claim 3, wherein said polyorganosilane containing a vinyl group, at least, in a part thereof is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane and tetravinylsilane.

Claim 5 (original): An organic insulating film according to Claim 1, wherein a C=C bond is contained.

Claim 6 (original): An organic insulating film according to Claim 5, wherein a vinyl group is contained.

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Claim 7 (currently amended): An organic insulating film according to ~~one of Claims~~ Claim 1, wherein said organic insulating film is one selected from the group consisting of a SiCH film, a SiCHN film and a SiOCH film.

Claim 8 (original): An organic insulating film according to Claim 7, wherein said SiCH film is composed of Si, C and H elements and a C/Si composition ratio thereof is not less than 0.9.

Claim 9 (original): An organic insulating film according to Claim 8, wherein said SiCH film has a density of less than 1.4 g / cm^3.

Claim 10 (original): An organic insulating film according to Claim 7, wherein said SiCHN film is composed of Si, C, H and N elements and a C/Si composition ratio thereof is not less than 1.0.

Claim 11 (original): An organic insulating film according to Claim 10, wherein said SiCHN film has a density of less than 1.6 g / cm^3.

Claim 12 (original): An organic insulating film according to Claim 7, wherein said SiOCH film is composed of, at least, Si, C, O and H elements and a C/Si composition ratio thereof is not less than 0.8.

Claim 13 (original): An organic insulating film according to Claim 12, wherein said SiOCH film has a density of less than 1.2 g / cm^3.

Claim 14 (original): A method of manufacturing an organic insulating film, wherein a film is grown by the plasma CVD (Chemical Vapor Deposition) method, and source gases are an oxidizing agent, an inert gas and a polyorganosilane whose C/Si ratio is, at least, equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

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Claim 15 (original): A method of manufacturing an organic insulating film according to Claim 14, wherein said inert gas is one selected from the group consisting of helium, argon and xenon.

Claim 16 (original): A method of manufacturing an organic insulating film according to Claim 14, wherein said oxidizing agent is one selected from the group consisting of O_2, O_3, H_2O, CO and CO_2.

Claim 17(original): A method of manufacturing an organic insulating film according to Claim 14, wherein said polyorganosilane is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane, tetravinylsilane, tetraethylsilane and triethylsilane.

Claim 18 (original): A method of manufacturing an organic insulating film according to Claim 14, wherein said polyorganosilane contains a vinyl group, at least, in a part thereof.

Claim 19 (original): A method of manufacturing an organic insulating film according to Claim 18, wherein said polyorganosilane containing a vinyl group, at least, in a part thereof is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane and tetravinylsilane.

Claim 20 (original): A method of manufacturing an organic insulating film according to Claim 14, wherein said organic insulating film is a SiOCH film composed of, at least, Si, C, H and O elements.

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Claim 21 (currently amended): A method of manufacturing an organic insulating film, wherein a film is grown by the plasma CVD method, and source gases are an inert gas that is one of helium, argon and xenon, and [[an]] a polyorganosilane whose C/Si ratio is, at least, equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 22 (original): A method of manufacturing an organic insulating film according to Claim 21, wherein said polyorganosilane is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane, tetravinylsilane, tetraethylsilane and triethylsilane.

Claim 23 (original): A method of manufacturing an organic insulating film according to Claim 21, wherein said polyorganosilane contains a vinyl group, at least, in a part thereof.

Claim 24 (original): A method of manufacturing an organic insulating film according to Claim 23, wherein said polyorganosilane containing a vinyl group, at least, in a part thereof is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane and tetravinylsilane.

Claim 25 (original): A method of manufacturing an organic insulating film according to Claim 21, wherein said organic insulating film is a SiCH film composed of Si, C and H elements.

Claim 26 (currently amended): A method of manufacturing an organic insulating film, wherein a film is grown by the plasma CVD method, and source gases are a nitrogen containing gas, an inert gas that is one of helium, argon and xenon, and [[an]] a polyorganosilane whose

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C/Si ratio is, at least, equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 27 (original): A method of manufacturing an organic insulating film, wherein said nitrogen containing gas is one of ammonia, N_2 and hydrazine.

Claim 28 (original): A method of manufacturing an organic insulating film according to Claim 26, wherein said polyorganosilane is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane, tetravinylsilane, tetraethylsilane and triethylsilane.

Claim 29 (original): A method of manufacturing an organic insulating film according to Claim 26, wherein said polyorganosilane contains a vinyl group, at least, in a part thereof.

Claim 30 (original): A method of manufacturing an organic insulating film according to Claim 29, wherein said polyorganosilane containing a vinyl group, at least, in a part thereof is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane and tetravinylsilane.

Claim 31 (original): A method of manufacturing an organic insulating film according to Claim 26, wherein said organic insulating film is a SiCHN film composed of Si, C, H and N elements.

Claim 32 (original): A semiconductor device comprising, at least, one insulating film selected from the group consisting of an interlayer insulating film, an etching stopper film and a barrier insulating film against a metal; wherein

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said interlayer insulating film, etching stopper film or barrier insulating film against a metal is an organic insulating film; wherein

said organic insulating film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 33 (original): A semiconductor device according to Claim 32, which comprises a trench interconnection structure.

Claim 34 (original): A semiconductor device having a trench interconnection structure, which comprises a first insulating film formed on a semiconductor substrate, a first trench interconnection formed in said first insulating film, a second insulating film, a third insulating film, a second trench interconnection formed in said third insulating film, a via plug that is formed in said second insulating film and connects said first trench interconnection with said second trench interconnection; wherein

at least said first insulating film, said second insulating film and said third insulating film are each made of a SiOCH film as set forth in Claim 7.

Claim 35 (original): A semiconductor device according to Claim 34, wherein said first insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 36 (original): A semiconductor device according to Claim 34; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

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Claim 37 (original): A semiconductor device according to Claim 34; wherein

said second insulating film is a layered film made of a barrier insulating film, a SiOCH film as set forth in Claim 7 and a hard mask film; and

said barrier insulating film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 38 (original): A semiconductor device according to Claim 34; wherein

said second insulating film is a layered film made of a barrier insulating film and said SiOCH film; and

said barrier insulating film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 39 (original): A semiconductor device according to Claim 34; wherein

said second insulating film is a layered film made of a barrier insulating film, said SiOCH film and an etching stopper film; and

each of said barrier insulating film and said etching stopper film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 40 (original): A semiconductor device according to Claim 34, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 41 (original): A semiconductor device according to Claim 34; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

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Claim 42 (original): A semiconductor device according to Claim 34; wherein

a top section of said second trench interconnection is covered with a barrier insulating film; and

said barrier insulating film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 43 (currently amended): A semiconductor device according to Claim 36 ~~one of Claims 36, 39 and 41~~, wherein said etching stopper film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 44 (currently amended): A semiconductor device according to Claim 37 ~~one of Claims 37, 38, 39 and 42~~, wherein said barrier insulating film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 45 (original): A semiconductor device according to Claim 34, wherein, at least, one of said trench interconnection and said via plug is formed of a copper containing metal.

Claim 46 (original): A semiconductor device according to Claim 45, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

Claim 47 (original): A semiconductor device according to Claim 34, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

Claim 48 (original): A method of manufacturing a semiconductor device which comprises, at least, one insulating film selected from the group consisting of an interlayer insulating film, an etching stopper film and a barrier insulating film against a metal; wherein

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said interlayer insulating film, etching stopper film or barrier insulating film against a metal is an organic insulating film ;wherein

said organic insulating film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100 ;wherein

said organic insulating film is one selected from the group consisting of a SiCH film, a SiCHN film and a SiOCH film.

Claim 49 (original): A method of manufacturing a semiconductor device according to Claim 48, wherein said semiconductor device comprises a trench interconnection structure.

Claim 50 (original): A method of manufacturing a semiconductor device having a trench interconnection structure; which comprises the steps of:

forming a first insulating film on a semiconductor substrate;

etching said first insulating film selectively and thereby forming a first interconnection trench pattern;

filling up said first interconnection trench pattern with a metal to form a first trench interconnection;

forming a second insulating film;

etching said second insulating film selectively and thereby forming a via hole to reach the top face of said first trench interconnection;

filling up said via hole with a metal to form a via plug;

forming a third insulating film;

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etching said third insulating film selectively and thereby forming a second interconnection trench pattern so that at least a part thereof may reach the top face of said via plug;

filling up said second interconnection trench pattern with a metal to form a second trench interconnection; and

forming a barrier insulating film; wherein

at least one insulating film selected from the group consisting of said first, second and third insulating films is made of a SiOCH film; wherein

said SiOCH film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 51 (original): A method of manufacturing a semiconductor device according to Claim 50, wherein

said first insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 52 (original): A method of manufacturing a semiconductor device according to Claim 50; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of said SiCH film and said SiCHN film; wherein

said SiCH and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

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Claim 53 (original): A method of manufacturing a semiconductor device according to Claim 50; wherein

said second insulating film is a layered film made of a barrier insulating film, said SiOCH film and a hard mask film; and

said barrier insulating film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 54 (original): A method of manufacturing a semiconductor device according to Claim 50, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 55 (original): A method of manufacturing a semiconductor device according to Claim 50; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 56 (original): A method of manufacturing a semiconductor device having a trench interconnection structure; which comprises the steps of:

forming a first insulating film on a semiconductor substrate;

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etching said first insulating film selectively and thereby forming a first interconnection trench pattern;

filling up said first interconnection trench pattern with a metal to form a first trench interconnection;

forming a second insulating film and a third insulating film;

etching said second insulating film and said third insulating film selectively and thereby forming a via hole to reach the top face of said first insulating film;

etching said third insulating film selectively and thereby forming a second interconnection trench to reach the top face of said second insulating film;

filling up said via hole and said second interconnection trench with a metal to form a via plug and a second trench interconnection; and

forming a fourth insulating film; wherein

at least one insulating film selected from the group consisting of said first, second and third insulating films is made of a SiOCH film; wherein

said SiOCH film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 57 (original): A method of manufacturing a semiconductor device having a trench interconnection structure; which comprises the steps of:

forming a first insulating film on a semiconductor substrate;

etching said first insulating film selectively and thereby forming a first interconnection trench pattern;

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filling up said first interconnection trench pattern with a metal to form a first trench interconnection;

forming a second insulating film and a third insulating film;

etching said third insulating film selectively and thereby forming a second interconnection trench to reach the top face of said second insulating film;

etching a part of a bottom section of said second interconnection trench selectively and thereby forming a via hole to reach the top face of said first insulating film;

filling up said via hole and said second interconnection trench with a metal to form a via plug and a second trench interconnection; and

forming a fourth insulating film; wherein

at least one insulating film selected from the group consisting of said first, second and third insulating films is made of a SiOCH film; wherein

said SiOCH film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 58 (original): A method of manufacturing a semiconductor device according to Claim 56, wherein said first insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 59 (original): A method of manufacturing a semiconductor device according to Claim 57, wherein said first insulating film is a layered film made of said SiOCH film and a hard mask film.

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Claim 60 (original): A method of manufacturing a semiconductor device according to Claim 56; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film: wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 61 (original): A method of manufacturing a semiconductor device according to Claim 57; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film: wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 62 (original): A method of manufacturing a semiconductor device according to Claim 56; wherein

said second insulating film is a layered film made of a barrier insulating film and said SiOCH film; and

said barrier insulating film is either of a SiCH film and a SiCHN film; wherein

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said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 63 (original): A method of manufacturing a semiconductor device according to Claim 57; wherein

said second insulating film is a layered film made of a barrier insulating film and said SiOCH film; and

said barrier insulating film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 64 (original): A method of manufacturing a semiconductor device according to Claim 56; wherein

said second insulating film is a layered film made of a barrier insulating film, said SiOCH film and an etching stopper film; and

each of said barrier insulating film and said etching stopper film is either of a SiCH film and a SiCHN film ; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 65 (original): A method of manufacturing a semiconductor device according to Claim 57; wherein

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said second insulating film is a layered film made of a barrier insulating film, said SiOCH film and an etching stopper film; and

each of said barrier insulating film and said etching stopper film is either of a SiCH film and a SiCHN film ; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 66 (original): A method of manufacturing a semiconductor device according to Claim 56, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 67 (original): A method of manufacturing a semiconductor device according to Claim 57, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 68 (original): A method of manufacturing a semiconductor device according to Claim 56; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

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Claim 69 (original): A method of manufacturing a semiconductor device according to Claim 57; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 70 (original): A method of manufacturing a semiconductor device having a trench interconnection structure; which comprises the steps of:

forming a first insulating film on a semiconductor substrate;

etching said first insulating film selectively and thereby forming a first interconnection trench pattern;

filling up said first interconnection trench pattern with a metal to form a first trench interconnection;

forming a second insulating film;

forming an etching stopper film;

making an opening selectively in said etching stopper film;

forming a third insulating film;

etching said third insulating film selectively so that a second interconnection trench to reach the top face of said second insulating film may be formed and, together therewith, forming a via hole to reach a top section of said first interconnection through said opening;

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filling up said via hole and said second interconnection trench with a metal to form a via plug and a second trench interconnection; and

forming a fourth insulating film; wherein

at least one insulating film selected from the group consisting of said first, second and third insulating films is made of a SiOCH film, and said etching stopper film is made of either of a SiCH film and a SiCHN film ; wherein

said SiOCH film, said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 71 (original): A method of manufacturing a semiconductor device according to Claim 70, wherein said first insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 72 (original): A method of manufacturing a semiconductor device according to Claim 70; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 73 (currently amended): A method of manufacturing a semiconductor device according to Claim 70; wherein

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said second insulating film is a layered film made of a barrier insulating film and said SiOCH film; and

said barrier insulating film is either of a SiCH film [[and]] or a SiCHN film; wherein

said SiCH film [[and]] or said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 74 (original): A method of manufacturing a semiconductor device according to Claim 70, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

Claim 75 (currently amended): A method of manufacturing a semiconductor device according to Claim 70; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film [[and]] or a SiCHN film; wherein

said SiCH film [[and]] or said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 76 (currently amended): A method of manufacturing a semiconductor device according to Claim 70; wherein said barrier insulating film is either of a SiCH film [[and]] or a SiCHN film; wherein

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said SiCH film [[and]] or said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

Claim 77 (original): A method of manufacturing a semiconductor device according to Claim 50, wherein at least one of said trench interconnection and said via plug is formed of a copper containing metal.

Claim 78 (currently amended): A method of manufacturing a semiconductor device according to ~~one of Claims~~ Claim 50, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

Claim 79 (currently amended): A method of manufacturing a semiconductor device according to ~~one of Claims~~ Claim 50, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

Claim 80 (original): A method of manufacturing a semiconductor device according to Claim 56, wherein at least one of said trench interconnection and said via plug is formed of a copper containing metal.

Claim 81 (currently amended): A method of manufacturing a semiconductor device according to ~~one of Claims~~ Claim 56, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

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Claim 82 (currently amended): A method of manufacturing a semiconductor device according to ~~one of Claims~~ Claim 57, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

Claim 83 (original): A method of manufacturing a semiconductor device according to Claim 57, wherein at least one of said trench interconnection and said via plug is formed of a copper containing metal.

Claim 84 (currently amended): A method of manufacturing a semiconductor device according to ~~one of Claims~~ Claim 57, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

Claim 85 (currently amended): A method of manufacturing a semiconductor device according to ~~one of Claims~~ Claim 57, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

Claim 86 (original): A method of manufacturing a semiconductor device according to Claim 64, wherein at least one of said trench interconnection and said via plug is formed of a copper containing metal.

Claim 87 (currently amended): A method of manufacturing a semiconductor device according to ~~one of Claims~~ Claim 64, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

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Claim 88 (currently amended): A method of manufacturing a semiconductor device according to ~~one of Claims~~ Claim 64, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

Claim 89 (new): A semiconductor device according to Claim 36, wherein said etching stopper film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 90 (new): A semiconductor device according to Claim 39, wherein said etching stopper film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 91 (new): A semiconductor device according to Claim 41, wherein said etching stopper film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 92 (new): A semiconductor device according to Claim 38, wherein said barrier insulating film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 93 (new): A semiconductor device according to Claim 39, wherein said barrier insulating film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

Claim 94 (new): A semiconductor device according to Claim 42, wherein said barrier insulating film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

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